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LSI Logic Corporation
Legal Department - IP
1621 Barber Lane, MS D-106
Milpitas, CA 95035Date September 16, 2005Number of pages including cover sheet 2

To: US PTO

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TC 1765

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From: Connie del Castillo

Intellectual Property Paralegal

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REMARKS:

☐ Urgent☐ For your review☒ Reply ASAP☐ Please commentApplication Number: 10/733,034Filing date: December 11, 2003First named inventor: Kunal Taravade et al.Attorney docket number: 01-916/1D / 1003-0637

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Kunal Taravade et. al.

Serial No. :

10/733,034

Filed :

December 11, 2003

For :

Method Of Fabricating An Integral
Capacitor And Gate Transistor
Having Nitride and Oxide Polish St
Layers Using Chemical Mechanical
Polishing Elimination

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§Group Art Unit :

1765

Examiner :

Huynh, Yennhu B.

Atty Docket :

1003-0637 / 01-916/1D

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STATUS REQUEST

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request a status of the above referenced application. Please mail the
status notification to the address stated below.

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Date: 14 Sept 05

Respectfully submitted,



Timothy Croll, Ph: [+1] 408-433-7191

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